IN THE SPECIFICATION

Replace the paragraph containing line 27 of page 13 with the following paragraph:

Specifically, if HDL Simulation Process 104 is a Verilog HDL simulator, then Instrumented HDL Source Code 103 contains calls through the Verilog HDL Programming Language Interface (or PLI) to the Monitoring Process 106, wherein the Monitoring Process 106 is a typically a program written in the C programming language. The Instrumented HDL Source Code 103 is provided with both specific textual function calls to Monitoring Process 106 (as permitted by the PLI), while Instrumentation Mapping Files 111 specify certain signals being indicated as callback nodes to Monitoring Process 106 (as also permitted by the PLI). Once the HDL Simulation Process 104 has invoked the Monitoring Process 106, Monitoring Process 106 is able to examine the value of nodes of the HDL Simulation Process 104 (also in the manner permitted by the PLI) in order to determine how observability-based code coverage is to proceed. This bidirectional communication between HDL Simulation Process 104 and Monitoring Process 106 is indicated by bidirectional PLI edge 110.

Delete the text on page 11, lines 19-24 (the section entitled "BRIEF DESCRIPTION OF THE APPENDIX").

Immediately below the last line of page 39, and before the first line of page 40, insert the text of the following 10 pages: